# Small Signal MOSFET

-20 V, -280 mA, P-Channel with ESD Protection, SOT-723

# Features

- Enables High Density PCB Manufacturing
- 44% Smaller Footprint than SC-89 and 38% Thinner than SC-89
- Low Voltage Drive Makes this Device Ideal for Portable Equipment
- Low Threshold Levels, 1.8 V R<sub>DS(on)</sub> Rating
- Low Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels Using the Same Basic Topology.
- This is a Pb–Free Device

## Applications

- Interfacing, Switching
- High Speed Switching
- Cellular Phones, PDA's

### **MAXIMUM RATINGS** (T<sub>J</sub> = $25^{\circ}$ C unless otherwise stated)

Parame	ter		Symbol	Value	Unit	
Drain-to-Source Voltage	V <sub>DSS</sub>	-20	V			
Gate-to-Source Voltage	te-to-Source Voltage					
Continuous Drain	Steady	$T_A = 25^{\circ}C$		-260		
Current (Note 1)	State	T <sub>A</sub> = 85°C	ID	-185	mA	
	t ≤ 5 s	T <sub>A</sub> = 25°C		-280		
Power Dissipation	Steady			400		
(Note 1)	State	T <sub>A</sub> = 25°C	PD		mW	
	t ≤ 5 s			500		
Continuous Drain		$T_A = 25^{\circ}C$	ID	-215	mA	
Current (Note 2)	Steady	T <sub>A</sub> = 85°C		-155	ШA	
Power Dissipation (Note 2)	State	$T_A = 25^{\circ}C$	P <sub>D</sub>	280	mW	
Pulsed Drain Current	t <sub>p</sub> =	10 μs	I <sub>DM</sub>	-310	mA	
Operating Junction and St	T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C			
Source Current (Body Diod	۱ <sub>S</sub>	-240	mA			
Lead Temperature for Solo (1/8" from case for 10 s)	lering Purp	ooses	ΤL	260	°C	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.

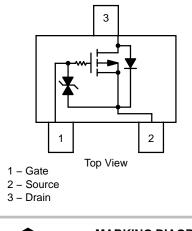


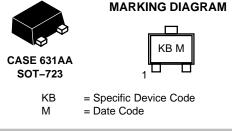
# **ON Semiconductor®**

### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> Max
	2.7 Ω @ –4.5 V	
–20 V	4.1 Ω @ –2.5 V	–280 mA
	6.1 Ω @ –1.8 V	

SOT-723 (3-LEAD)





# ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTK3142PT1G	SOT-723 (Pb-Free)	4000/Tape & Reel 4 mm Pitch
NTK3142PT5G	SOT-723 (Pb-Free)	8000/Tape & Reel 2 mm Pitch

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Мах	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{ hetaJA}$	315	
Junction-to-Ambient $- t = 5 s$ (Note 3)	$R_{ hetaJA}$	250	°C/W
Junction-to-Ambient - Steady State Minimum Pad (Note 4)	$R_{\thetaJA}$	440	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
Surface-mounted on FR4 board using the minimum recommended pad size.

#### **MOSFET ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 V$ , $I_D = -100 \mu A$		-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	$I_D = -100 \ \mu A$ , Reference to 25°C			14		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$ , $T_J = 25^{\circ}C$				-1	
		$V_{DS} = -16 V$	T <sub>J</sub> = 125°C			20	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 5 V$				±1	μΑ
ON CHARACTERISTICS (Note 5)							

Gate Threshold Voltage	V <sub>GS(TH)</sub>		-0.4		-1.3	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	$V_{GS} = V_{DS}, I_D = -250 \ \mu A$		-2.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(ON)</sub>	$V_{GS} = -4.5 V$ , $I_D = -260 mA$		2.9	4.0	Ω
Drain-to-Source On Resistance	R <sub>DS(ON)</sub>	$V_{GS} = -4.5V, I_D = -10 \text{ mA}$		2.7	3.4	
		$V_{GS} = -2.5 \text{ V}, \text{ I}_{D} = -1 \text{ mA}$		4.1	5.3	Ω
		$V_{GS} = -1.8 \text{ V}, \text{ I}_{D} = -1 \text{ mA}$		6.1	10	
Forward Transconductance	9fs	$V_{DS} = -5 V$ , $I_{D} = -10 mA$		73		mS

#### CAPACITANCES

Input Capacitance	C <sub>ISS</sub>		15.3	
Output Capacitance	C <sub>OSS</sub>	$V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = -10 V	4.3	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>		2.3	

# SWITCHING CHARACTERISTICS, $V_{GS}$ = 4.5 V (Note 6)

Turn-On Delay Time	t <sub>d(ON)</sub>		8.4	16	
Rise Time	t <sub>r</sub>	$V_{GS} = -4.5 \text{ V}, V_{DD} = -5 \text{ V}, I_D = -100 \text{ mA},$	15.3	28	ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$R_{G} = 6 \Omega$	37.5	80	115
Fall Time	t <sub>f</sub>		22.7	43	

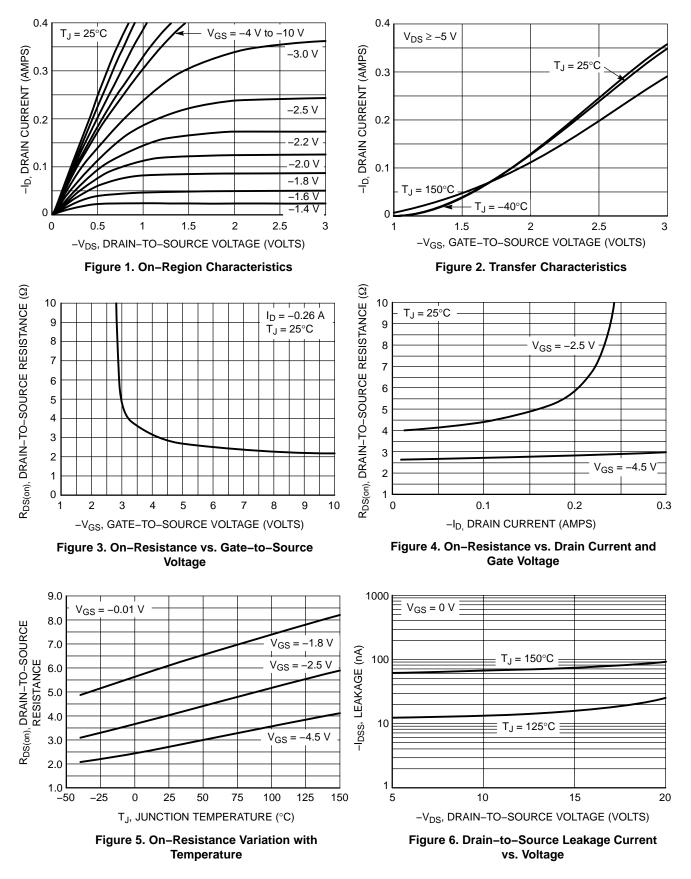
#### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –10 mA	$T_J = 25^{\circ}C$	0.69	-1.2	V
		VGS = 0 V, IS= = 10 IIIA	T <sub>J</sub> = 125°C	0.56		v
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = -20 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = -1.0 A		37	80	
Charge Time	t <sub>a</sub>			15.9	30	ns
Discharge Time	t <sub>b</sub>			21.1	50	
Reverse Recovery Charge	Q <sub>RR</sub>			20	70	nC

5. Pulse Test: pulse width  $\leq$  300 µs, duty cycle  $\leq$  2%.

6. Switching characteristics are independent of operating junction temperatures.

# **TYPICAL PERFORMANCE CURVES**



#### 30 1000 $T_J = 25^{\circ}C$ $V_{GS} = 0 V$ $V_{DD} = -5 V$ $I_{\rm D} = -10 \, {\rm mA}$ 25 $V_{GS} = -4.5 V$ C, CAPACITANCE (pF) 20 100 $\dot{C}_{\text{iss}}$ t, TIME (ns) t<sub>d(off)</sub> 15 t<sub>d(on)</sub> 10 10 tr $\mathsf{C}_{\text{oss}}$ 5 Crss 0 1 0 2.5 5 7.5 10 12.5 15 17.5 20 1 10 100 -DRAIN-TO-SOURCE VOLTAGE (V) R<sub>G</sub>, GATE RESISTANCE (OHMS) Figure 7. Capacitance Variation Figure 8. Resistive Switching Time Variation vs. Gate Resistance



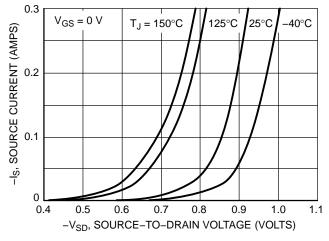
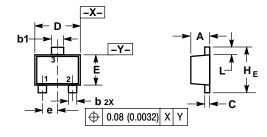


Figure 9. Diode Forward Voltage vs. Current

#### PACKAGE DIMENSIONS

SOT-723 CASE 631AA-01 ISSUE B



NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI V44.5M 1022

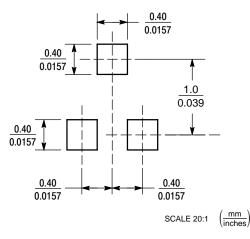
- Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETERS.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL
- THICKNESS OF BASE MATERIAL. 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	мі	LIMETE	RS	INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.45	0.50	0.55	0.018	0.020	0.022	
b	0.15	0.21	0.27	0.0059	0.0083	0.0106	
b1	0.25	0.31	0.37	0.010	0.012	0.015	
С	0.07	0.12	0.17	0.0028	0.0047	0.0067	
D	1.15	1.20	1.25	0.045	0.047	0.049	
Е	0.75	0.80	0.85	0.03	0.032	0.034	
е		0.40 BS	SC	0.016 BSC			
ΗE	1.15	1.20	1.25	0.045	0.047	0.049	
L	0.15	0.20	0.25	0.0059	0.0079	0.0098	

STYLE 3: PIN 1. ANODE 2. ANODE

3. CATHODE

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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